PS200
Data Sheet

PowerSmart® Configurable Battery Charger

PS200

PowerSmart® Configurable Battery Charger

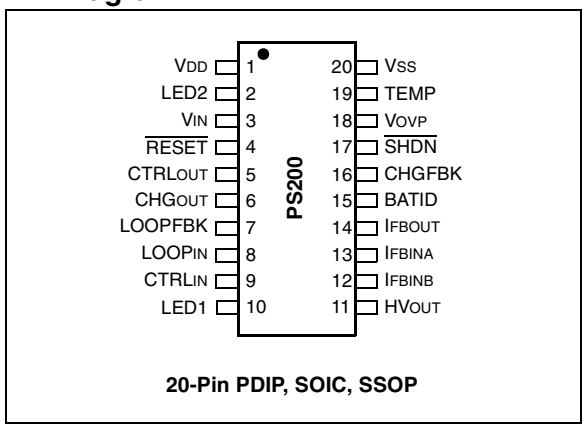
Features

- User configurable battery charger.
- Firmware available for the following cell chemistries:
  - Lithium Ion/Polymer (available now)
  - NiMH, NiCd (available Q2 2005)
  - Pb Acid (available Q3 2005)
- 10-bit ADC for voltage, current and temperature measurement:
  - Accurate Voltage Regulation (+/-1%)
  - Accurate Current Regulation (+/-5%)
- Maximum integration for optimal size:
  - Integrated voltage regulator
  - Internal 8 MHz clock oscillator
  - High-Frequency Switch mode charging – configurable switching frequency up to 1 MHz
- 256 bytes EEPROM storage for charging parameters
- Switch mode charger supports buck and synchronous buck topologies
- Configurable charge status display via two LEDs
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Power-saving Sleep mode

Applications

- Notebook Computers
- Personal Data Assistants
- Cellular Telephones
- Digital Still Cameras
- Camcorders
- Portable Audio Products
- Bluetooth® Devices
- Flashlights
- Power Tools

Pin Diagram



20-Pin PDIP, SOIC, SSOP

Pinout Description

Pin	Pin Name	Pin Type	Input Type	Output Type	Description
1	VDD	Supply	Power	—	Supply voltage
2	LED2	O	—	CMOS	Status indicator
3	VIN	I	Analog	—	Battery voltage input
4	$\overline{\text{RESET}}$	I	ST	—	Reset
5	CTRLOUT	O	—	CMOS	PWM output for setting current level
6	CHGOUT	O	—	CMOS	PWM output to a buck converter for charge control
7	LOOPFBK	I	Analog	—	Current feedback loop
8	LOOPIN	I	Analog	—	Current feedback loop input
9	CTRLIN	I	Analog	—	Current level control
10	LED1	O	—	CMOS	Status indicator
11	HVOUT	O	—	HVOD	High-voltage, open-drain output pin (optional)
12	IFBINB	I	Analog	—	Current feedback input pin B used for current scaling
13	IFBINA	I	Analog	—	Current feedback input pin A used for current scaling
14	IFBOUT	O	—	Analog	Current feedback output
15	BATID	I	Analog	—	Battery ID select
16	CHGFBK	I	Analog	—	Charge control feedback
17	$\overline{\text{SHDN}}$	O	—	Analog	Shutdown signal, active-low
18	VOVP	I	Analog	—	Overvoltage protection
19	TEMP	I	Analog	—	Battery temperature input
20	VSS	Supply	Power	—	Supply ground

Legend: I = Input, O = Output, ST = Schmitt Trigger Input Buffer, HVOD = High-Voltage Open-Drain

1.0 PS200 OVERVIEW

The PS200 is a configurable Switch mode charger which is comprised of a PIC16F microcontroller core and precision analog circuitry. This section explores the hardware features in relation to generic Switch mode charging. Subsequent sections will describe the operation of the PS200 with firmware for Lithium-based (**Section 2.0 "Lithium Chemistry Algorithm"**), Nickel-based (**Section 3.0 "Nickel Chemistry Algorithm"**) and Lead Acid (**Section 4.0 "Lead Acid Chemistry Algorithm"**) charging.

- Oscillator
- Power-saving Sleep mode
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- High-Endurance Flash/EEPROM Cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM retention: > 40 years
- High-Speed Comparator module with:
  - Two independent analog comparators
- Operational Amplifier module with two independent op amps
- Two-Phase Asynchronous Feedback PWM
- Voltage Regulator
- 10-bit (9-bit plus sign) A/D Converter
- In-Circuit Serial Programming™ (ICSP™) via two pins

1.1 Hardware Features

The PS200 features are well-suited for Switch mode battery charging. The PS200 device's block diagram (Figure 1-1) is to be used in conjunction with the Switch mode charger example (Figure 2-3, page 12).

- Current/Voltage Measurement Block – The Current/Voltage Measurement Block consists of a 10-bit Analog-to-Digital converter, operational amplifiers and a comparator. The output of this block is fed into the Charge Control module. Please refer to Figure 1-1.

  The inputs into this block are to be connected as described in Figure 2-3. The following signals are inputs into this block:
  - LOOPFBK – to comparator
  - LOOPIN – to op amp and ADC
  - CTRLIN – to op amp
  - IFBINB – to op amp
  - IFBINA – to op amp
  - BATID – to ADC
  - TEMP – to ADC
  - CHGFBK – to comparator

  The following signals are outputs from this block:
  - IFBOUT – from op amp
- Charge Control Module:
  - The charge control module generates a Pulse-Width Modulated signal called CHGOUT. Its frequency is configurable and can be set up to 1 MHz. This signal is connected to an external DC/DC buck converter.
- Voltage Regulator
  - The integrated voltage regulator is designed to work with unregulated DC supplies.
  - There are guidelines that should be followed. A series limiting resistor (RVDD) should be placed between the unregulated supply and the VDD pin. The value for this series resistor (RVDD) must be between RMIN and RMAX as shown in the following equation:

EQUATION 1-1:

$$R_{MAX} = \frac{Vs(MIN) - 5V) * 1000}{1.05 * (16\ mA + I(led))}$$

$$R_{MIN} = \frac{Vs(MAX) - 5V) * 1000}{.95 * (50\ mA)}$$

Where:

RMAX = maximum value of series resistor (ohms)
RMIN = minimum value of series resistor (ohms)

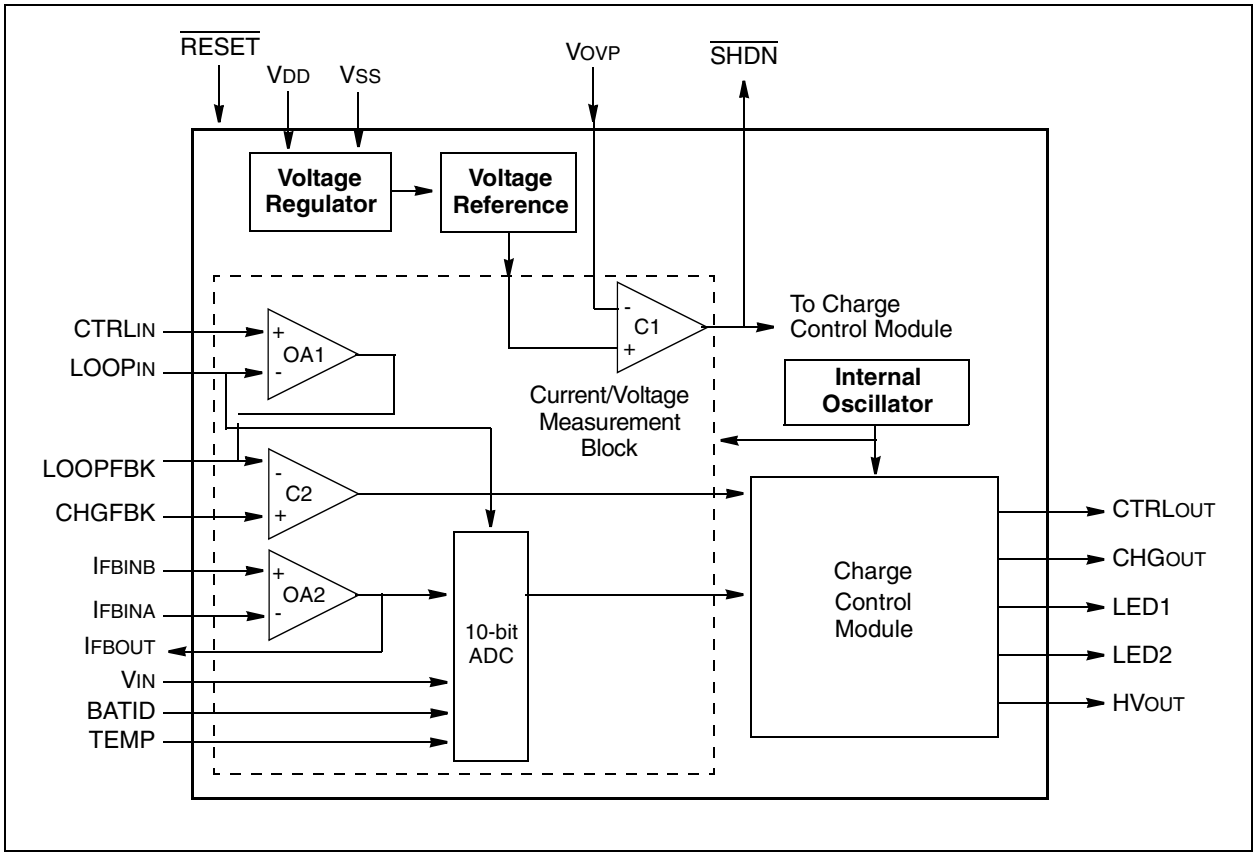
Vs(MIN) = minimum value of charger DC supply (VDC)
Vs(MAX) = maximum value of charger DC supply (VDC)

I(led) = total current drawn by all LEDs when illuminated simultaneously

The 1.05 and .95 constants are included to compensate for the tolerance of 5% resistors. The 16 mA constant is the anticipated load presented by the PS200, including the loading due to external components and a 4 mA minimum current for the shunt regulator itself. The 50 mA constant is the maximum acceptable current for the shunt regulator.

- The precision internal 8 MHz clock oscillator eliminates the need for external oscillator circuits.
- In-circuit configurability utilizing 256 bytes of on-board EEPROM.
- Power on Reset – The POR insures the proper start-up of the PS200 when voltage is applied to VDD.
- Brown-out Reset – The BOR is activated when the input voltage falls to 2.1V; the PS200 is reset.

FIGURE 1-1: PS200 BLOCK DIAGRAM



2.0 LITHIUM CHEMISTRY ALGORITHM

The PS200 provides an unprecedented level of configurability for charging Lithium Ion/Lithium Polymer battery packs. It's precision, 10-bit Analog-to-Digital converter and high-frequency Pulse-Width Modulator enable the PS200 to provide optimum control of charging algorithms for lithium battery chemistries. Special features include an internal voltage regulator and an internal clock oscillator that reduce external component count.

2.1 Lithium Overview

2.1.1 MULTI-STEP CHARGING

To ensure the proper treatment of lithium chemistries during extreme temperature and voltage conditions, multi-step charging is required. The PS200 starts the charging cycle upon sensing the presence of a battery pack and a valid charging supply. During charge qualification, the battery's temperature and voltage are measured to determine the appropriate initial state. The initial states include Charge Suspend, Precharge and Current Regulation. Charge Suspend halts charging when the user defined preset conditions for charging are not met. Precharge allows for the recovery of deeply discharged batteries by applying a low-charge current. Current Regulation provides constant current, voltage limited charge. Upon reaching the target voltage during Current Regulation, the Voltage Regulation state is entered. Charging continues at a constant voltage until the current decreases to the user specified minimum current threshold (VRIMin). At this threshold, charging is terminated and the End-Of-Charge state is reached.

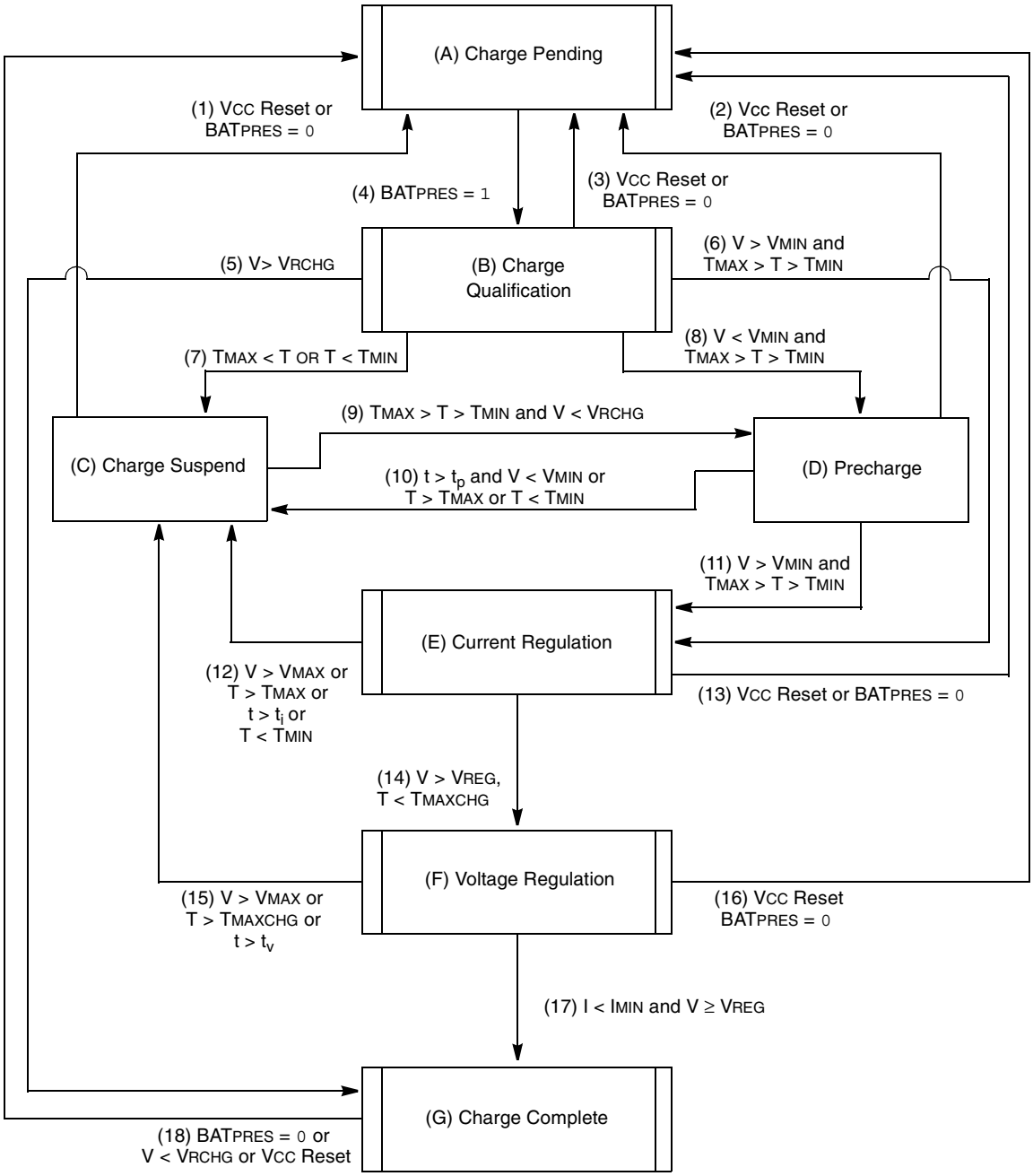
The state diagram illustrates the charging cycle (see Figure 2-1).

2.1.2 USER CONFIGURABLE PARAMETERS

The PS200 supports user configurable parameters that allow for customizing the charging profile. This feature allows for the maximum reuse of hardware, thus reducing time-to-market. These parameters include:

- Battery Temperature:
  - Minimum/maximum temperature for charge initiation
  - Maximum temperature allowed during charge
- Battery Voltage:
  - Minimum/maximum voltage for charge initiation
  - Target voltage during Voltage Regulation
  - Voltage at which the charger will restart charging after completion of a valid charge cycle
- Charge Current:
  - Target current during Current Regulation
  - Taper current threshold for End-Of-Charge during Voltage Regulation
  - Target current during Precharge
- Time:
  - Precharge time limit
  - Current Regulation time limit
  - Voltage Regulation time limit
- Status Display:
  - Two LEDs denote the charge states. Their flash rates can be modified.

FIGURE 2-1: PS200 STATE DIAGRAM LI CHARGER



Legend:

T	=	battery temperature	I	=	charge current
TMIN	=	minimum temperature allowed during charging	IMIN	=	taper current threshold for End-Of-Charge during voltage regulation
TMAX	=	maximum temperature allowed during charging			
TMAXCHG	=	maximum temperature allowed during voltage regulation	t	=	time
V	=	battery voltage	t_p	=	precharge time limit
VMIN	=	minimum voltage for entering current regulation	t_i	=	current regulation time limit
VMAX	=	maximum voltage for charge initiation	t_v	=	voltage current time limit
VREG	=	target voltage during charge regulation	BATPRES	=	battery present variable; if '1', then battery is present; if '0', then battery is not present
VRCHG	=	voltage threshold at which charging will restart			

Note: When the PS200 resets, it enters the Charge Pending state.

2.2 Lithium Charging

To ensure the proper treatment of lithium chemistries during extreme temperature and voltage conditions, multi-step charging is required. The PS200 measures key voltage, temperature and time parameters. It compares them to user defined voltage, temperature and time limits. These limits are described in **Section 2.4 "Lithium Configurable Parameters"**.

Note:	Refer to Figure 2-1 and Figure 2-2 for clarification when reading this section.

2.2.1 CHARGE PENDING STATE – BEGINNING THE CHARGE CYCLE

The PS200 is initially set in the Charge Pending state (A). In this state, the presence of a battery pack must be sensed in order to begin the charging cycle. The PS200 comes up in the Charge Pending state, after a Reset, independent of the previous state.

2.2.2 CHARGE QUALIFICATION STATE

During charge qualification, the battery's temperature and voltage are measured to determine the next charging state. There are four possible next states (see Figure 2-1).

1. If the battery's temperature is outside of the limits for charge initiation (TMAX, TMIN) then the next state is Charge Suspend (C).
2. If the battery's voltage is less than the minimum voltage for charge initiation (VMIN) and its temperature is within the limits for charge initiation (TMAX, TMIN), then the next state is Precharge (D).
3. If the battery's voltage is above the minimum voltage for charge initiation (VMIN) and its temperature is within the limits for charge initiation (TMAX, TMIN), then the next state is Current Regulation (E).
4. If the battery's voltage is above the voltage at which charging will restart (VRCHG), then the next state is Charge Complete (G).

2.2.3 PRECHARGE STATE

The Precharge state allows for the recovery of a deeply discharged battery pack by applying a low charge rate. In this state, a user configured precharge current is applied to the battery, resulting in an increase in the battery's voltage (refer to Figure 2-2). There are three possible next states (see Figure 2-1).

1. If the battery's voltage is above the minimum voltage for charge initiation (VMIN) and the battery's temperature is within the limits for charge initiation (TMAX, TMIN), then the next state is Current Regulation (E).
2. If the Precharge state time limit is exceeded (t_p) and the battery's voltage remains less than the minimum voltage for charge initiation (VMIN), then the next state is Charge Suspend (C).

   If the Precharge state time limit is exceeded (t_p) and the battery's temperature is greater than the maximum temperature for charge initiation (TMAX), then the next state is Charge Suspend (C).

   If the Precharge state time limit is exceeded (t_p) and the battery's temperature is less than the minimum temperature for charge initiation (TMIN), then the next state is Charge Suspend (C).
3. If the battery pack is taken away (BATPRES = 0), then the PS200 enters the Charge Pending (A) state.

2.2.4 CHARGE SUSPEND STATE

In the Charge Suspend state, no current is applied to the battery pack. There are two possible next states (see Figure 2-1).

1. If the battery's temperature is within the limits for charge initiation (TMAX, TMIN) and its voltage is less than the voltage at which charging would restart (VRCHG), then the next state is Precharge (D).
2. If the battery pack is taken away (BATPRES = 0), then the PS200 enters the Charge Pending (A) state.

2.2.5 CURRENT REGULATION STATE

The Current Regulation state can be entered from the Precharge state or Charge Qualification state. Battery charging is initiated. This state provides constant current, voltage limited charging (refer to Figure 2-2). The charge current is referred to as IREG or the regulation current. While the current is applied, the battery's voltage increases until it reaches a voltage limit referred to as VREG or regulation voltage. Charging continues, during which battery voltage and temperature are monitored. There are three possible next states.

1. If the battery's voltage reaches or exceeds the voltage limit, VREG and its temperature remains below the maximum allowable during current regulated charging (TMAXCHG), then the next state is Voltage Regulation (F).
2. If the battery exhibits any one of the following conditions then the next state is Charge Suspend (C):
   - Battery voltage exceeds upper voltage limit for charging (VMAX)
   - Battery temperature exceeds upper temperature limit for charging (TMAX)
   - Battery temperature is below the lower temperature limit for charging (TMIN)

   If the time in the Current Regulation state exceeds the time limit (t_i), then the next state is Charge Suspend (C).
3. If the battery pack is taken away (BATPRES = 0), then the PS200 enters the Charge Pending (A) state.

2.2.6 VOLTAGE REGULATION STATE

Voltage Regulation provides charging at a constant voltage while the charge current decreases (or tapers) to the user specified minimum current threshold (IMIN). There are three possible next states.

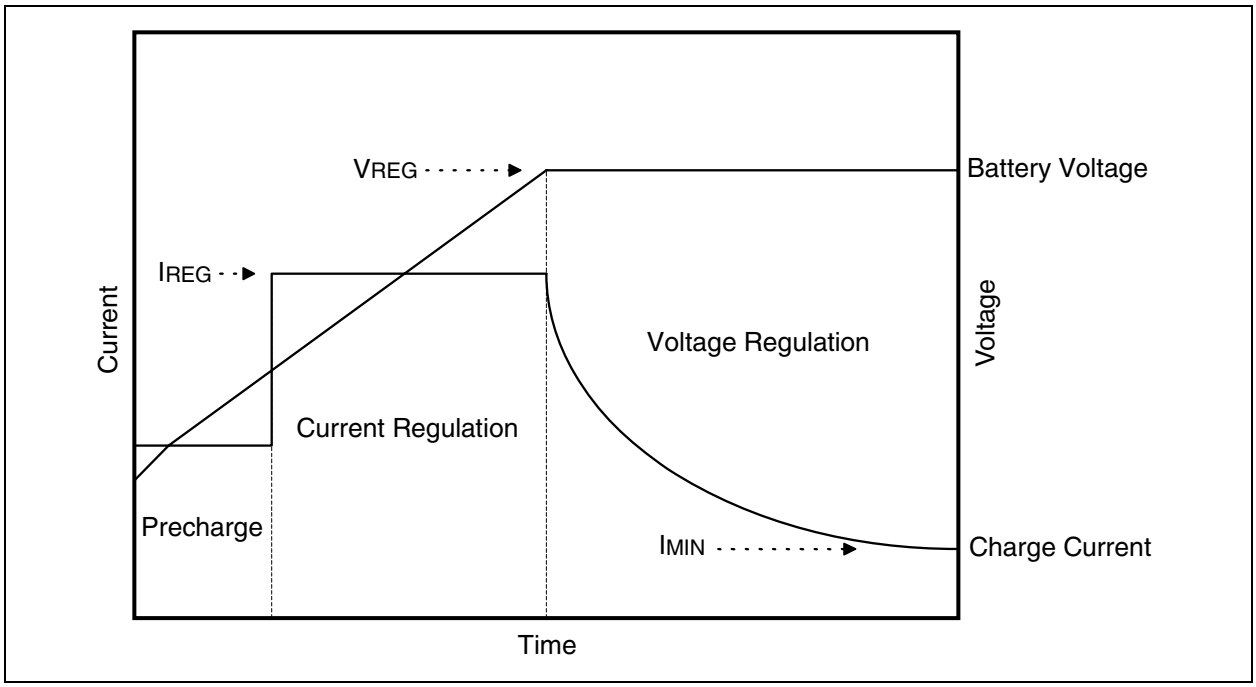
1. When the charge current reaches the taper current threshold for End-Of-Charge (IMIN) and the battery's voltage remains at the regulated voltage value (VREG), then the battery has reached the Charge Complete (G) state.
2. If the battery exhibits any one of the following conditions, then the next state is Charge Suspend (C).
   - Battery voltage exceeds upper voltage limit for charging (VMAX)
   - Battery temperature exceeds upper temperature limit for charging (TMAXCHG)

   If the time in the Voltage Regulation state exceeds the time limit (t_v), then the next state is Charge Suspend (C).
3. If the battery pack is taken away (BATPRES = 0), then the PS200 enters the Charge Pending (A) state.

2.2.7 CHARGE CYCLE COMPLETE STATE

The user specified minimum current threshold (IMIN) can be configured for various charging temperatures. At this threshold, charging is terminated and the End-Of-Charge state is reached. The PS200 can renew the charge cycle by entering the Charge Pending (A) state when: 1) the battery is removed (BATPRES = 0), or 2) if the battery's voltage falls below the recharge threshold voltage (VRCHG).

FIGURE 2-2: PS200 CHARGING PROFILE



2.3 KEELOQ® Algorithm

The PS200 includes Microchip's KEELOQ decoder algorithm. The KEELOQ code hopping technology is a worldwide standard providing a simple, yet highly secure, solution for authentication. Microchip's battery management products include the KEELOQ algorithm to provide secure identification for rechargeable batteries. When the KEELOQ algorithm is enabled, the PS200 will issue a 32-bit challenge to the attached rechargeable battery. The battery, which also includes the KEELOQ decoder algorithm, will generate a response. See Microchip application note *AN827 "Using KEELOQ® to Validate Subsystem Compatibility"* (DS00827) for details on implementing a complete KEELOQ battery authentication system.

2.4 Lithium Configurable Parameters

The PS200 device's configurable parameters allow for flexible changes in designing battery chargers. The parameters are categorized as follows:

- Configuration
- Charging Limits
  - Precharge
  - Current Regulation
  - Voltage Regulation
- LED Display Configuration

Please refer to Table 2-1 "PS200 Lithium Configurable Parameters".

2.4.1 CONFIGURATION PARAMETERS

The configuration parameters provide an identity to the battery pack and provide its basic characteristics to the PS200.

2.4.2 CHARGING LIMITS

2.4.2.1 Precharge Parameters

The Precharge parameters configure the charger's operation during this initial battery charging phase.

2.4.2.2 Current Regulation Parameters

The Current Regulation parameters configure the charger's operation during this second battery charging phase.

2.4.2.3 Voltage Regulation Parameters

The Voltage Regulation parameters configure the charger's operation during this third battery charging phase.

2.4.3 LED DISPLAY CONFIGURATION

The PS200 supports a two-LED charging state display. These LEDs can be configured to identify seven unique charger states:

- Charge Pending – charger is waiting for battery pack that needs charge.
- Charge Qualification – charger is determining if the battery pack can be safely charged.
- Precharge – charger is charging the battery pack under the conditions configured for precharge.
- Charge Suspend – charger has temporarily suspended charging the battery pack. This state is usually entered as a result of violating a maximum temperature requirement. Charging will resume when conditions are within required charging parameter values.
- Current Regulation – charger is charging the battery pack with a constant current.
- Voltage Regulation – charger is charging the battery pack at the constant target voltage.
- Charge Complete – charger has completed charging the battery pack.

TABLE 2-1: PS200 LITHIUM CONFIGURABLE PARAMETERS

Step 1 – Configuration					
Parameter Name	**# Bytes**	**Lower Limit**	**Upper Limit**	**Typical Value**	**Description**
MfgName	—	N/A	N/A	Microchip	ASCII value.
DevName	—	N/A	N/A	PS200	ASCII value.
SeriesCells	1	1	255	4	Number of series connected cells in the battery pack.
Capacity (mAh)	2	0	65535	2000	Full-charge capacity of the battery pack.
PWMFreq	1	7	83	15	LUT value which determines the PWM frequency.
Step 2 – Charging Limits					
Parameter Name	**# Bytes**	**Lower Limit**	**Upper Limit**	**Typical Value**	**Description**
PCVMin (mV)	2	0	65535	2500	Minimum cell voltage required to enable charging with precharge conditions.
PCVMax (mV)	2	0	65535	3000	Maximum cell voltage required to enable charging with precharge conditions.
PCCurrent (mA)	2	0	65535	200	Charging current during precharge.
PCTempMin	1	0	255	50	Minimum temperature required to enable charging with precharge conditions. PCTempMin value = (temperature °C * 10 + 200)/4; so typical value of 50 = 0°C.
PCTempMax	1	0	255	175	Maximum temperature required to enable charging with precharge conditions. PCTempMax value = (temperature °C * 10 + 200)/4; so typical value of 175 = 50°C.
PCTime (min)	1	0	255	60	Duration of precharge.
CRVTarg (mV)	2	0	65535	4200	Target cell voltage in current regulation. This is set to the fully charged voltage of one cell, typically, as specified by the cell manufacturer.
CRCurrent (mA)	2	0	65536	2000	Charging current during current regulation.
CRTimeMax (min)	1	0	255	90	Current regulation time limit.
VRVrech (mV)	2	0	65536	3780	Voltage regulation recharge cell voltage. Charger will automatically begin charging if cell voltage of pack falls below SeriesCells * VRVrech.
VRIMin (mA)	2	0	65536	150	Voltage regulation fully charged current. This is the value of the taper current or IMIN which will determine that the battery is fully charged.
VRTimeMax (min)	1	0	255	90	Voltage regulation time limit.
TempMax	1	0	255	200	Maximum temperature required to enable charging during current regulation and voltage regulation. TempMax value = (temperature °C * 10 + 200)/4; so typical value of 200 = 60°C.

TABLE 2-1: PS200 LITHIUM CONFIGURABLE PARAMETERS (CONTINUED)

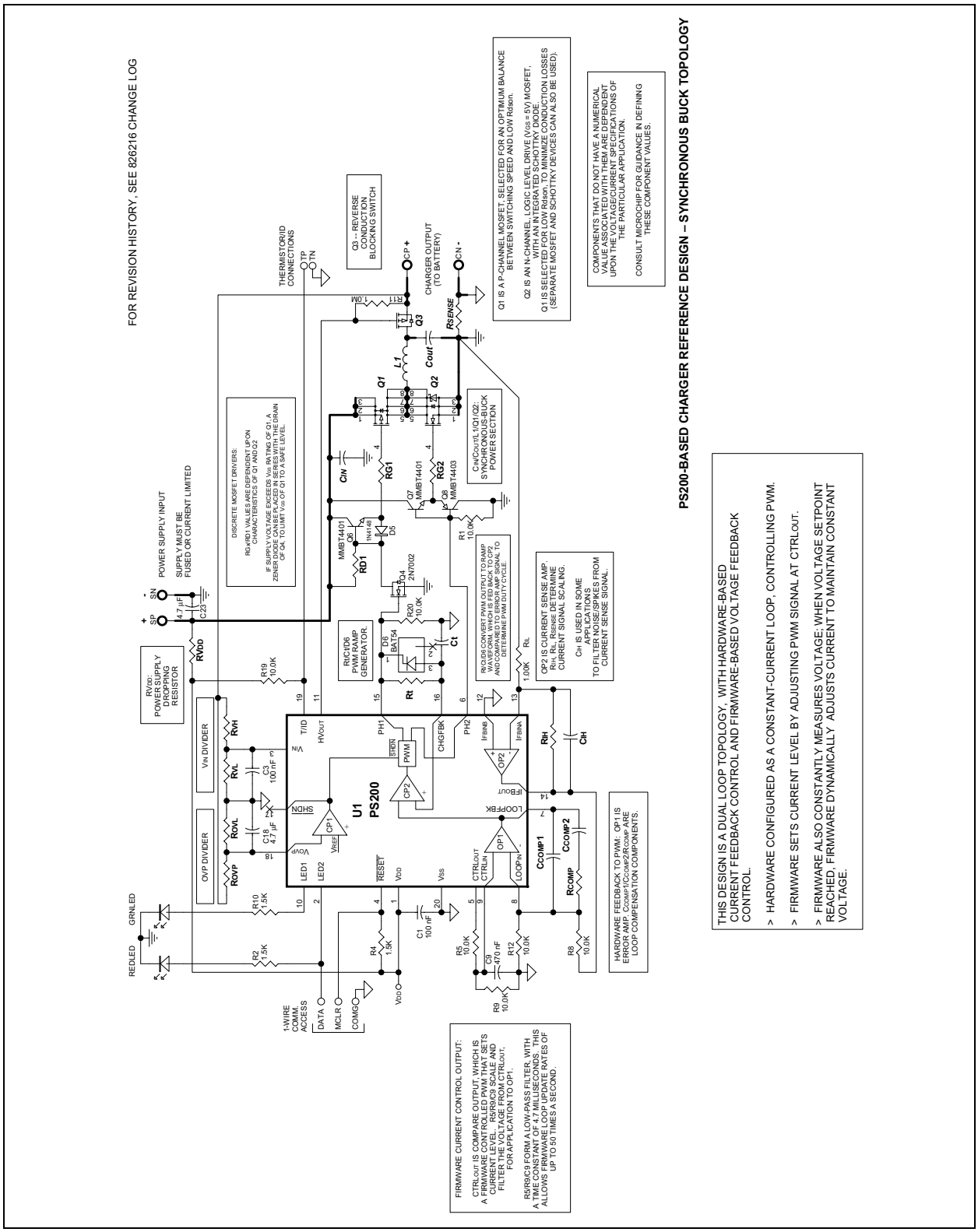
Step 3 – LED Display					
Parameter Name	**# Bytes**	**Lower Limit**	**Upper Limit**	**Typical Value**	**Description**
LED1Pending	1	N/A	N/A	0b00000000	LED1 display when charge is pending.
LED2Pending	1	N/A	N/A	0b00000000	LED2 display when charge is pending.
LED1Qual	1	N/A	N/A	0b00000000	LED1 display during charge qualification.
LED2Qual	1	N/A	N/A	0b00000000	LED2 display during charge qualification.
LED1PC	1	N/A	N/A	0b00000000	LED1 display during precharge.
LED2PC	1	N/A	N/A	0b00000000	LED2 display during precharge.
LED1Suspend	1	N/A	N/A	0b00000000	LED1 display when charge has been temporarily suspended.
LED2Suspend	1	N/A	N/A	0b00000000	LED2 display when charge has been temporarily suspended.
LED1CR	1	N/A	N/A	0b00000000	LED1 display during charge regulation.
LED2CR	1	N/A	N/A	0b00000000	LED2 display during charge regulation.
LED1VR	1	N/A	N/A	0b00000000	LED1 display during voltage regulation.
LED2VR	1	N/A	N/A	0b00000000	LED2 display during voltage regulation.
LED1Full	1	N/A	N/A	0b00000000	LED1 display when battery is fully charged.
LED2Full	1	N/A	N/A	0b00000000	LED2 display when battery is fully charged.
Miscellaneous					
Parameter Name	**# Bytes**	**Lower Limit**	**Upper Limit**	**Typical Value**	**Description**
PatternID	2	0x0	0xFFFF	0x0	Pattern ID.
BatIDMin	1	0	255	0	BATID input pin value minimum.
BatIDMax	1	0	255	255	BATID input pin value maximum.

2.5 Lithium Application

Figure 2-3 is an example of the PS200 in a synchronous buck charger for Lithium Ion batteries. The sense resistor (RSENSE) is in a low side configuration.

Refer to the Microchip web site (www.microchip.com) for the latest Application Notes that reference this theory of operation and component values.

FIGURE 2-3: SWITCH MODE CHARGER CIRCUIT EXAMPLE



3.0 NICKEL CHEMISTRY ALGORITHM

The PS200 algorithms for NiMH and NiCd chemistries are currently being developed.

4.0 LEAD ACID CHEMISTRY ALGORITHM

The PS200 algorithms for lead acid chemistries are currently being developed.

NOTES:

5.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias ..... -40 to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3 to +6.5V
Voltage on $\overline{RESET}$ with respect to Vss ..... -0.3 to +13.5V
Voltage on HV_{OUT} with respect to Vss ..... 0V to +8.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) ..... 800 mW
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin ..... 250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD}) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA(2)
Maximum output current sourced by each Port ..... 50 mA(2)

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

2: Total source current must not exceed the shunt regulator capacity.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.1 Reliability Targets

The device must be designed to target the following reliability specifications:

ESD: ±4000V HBM ±400V MM all pins including V_{DD}, V_{SS}, $\overline{RESET}$

Latch-up: ±400 mA @ 125°C

5.2 Design Targets

The AC/DC specifications included in the following sections are preliminary specifications that we intend to publish at product introduction. As the product matures, we intend to expand the specifications. Therefore, design should try and meet the following extended V_{DD}/temperature targets:

1. Frequency of operation: DC – 4 MHz, V_{DD} = 2.0V – 5.5V, -40°C to 125°C
2. Frequency of operation: DC – 20 MHz, V_{DD} = 4.5V – 5.5V, -40°C to 125°C

5.3 DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001B D001C	VDD	Supply Voltage	2.0 4.5	— —	5.0 5.0	V V	FOSC <= 4 MHz FOSC > 4 MHz
D002	VDR	RAM Data Retention Voltage(1)	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	VDD Voltage required to initiate a Brown-out Detect	—	2.1	—	V	
D010S	IDD	Supply Current(2)	—	—	—	mA	VDD and current are constant due to shunt regulator.
D020	IPD	Power-Down Current(3)	—	2.9	TBD	nA	VDD = 5.0V, WDT disabled

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{RESET}}$ = VDD.

3: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD and VSS.

5.4 Shunt Regulator

TABLE 5-1: SHUNT REGULATOR SPECIFICATIONS

Shunt Regulator Specifications		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to +125°C				
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Shunt Voltage	VSHUNT	4.75	—	5.25	Volts	
Shunt Current	ISHUNT	4	—	50	mA	
Shunt Resistance	RSHUNT	—	—	3	Ω	
Settling Time*	TSETTLE	—	—	150	ns	To 1% of final value
Load Capacitance	CLOAD	0.01	—	10	µF	Bypass capacitor on VDD pin
Regulator Operating Current	ΔISNT	—	180	—	µA	Includes band gap reference current

* These parameters are characterized but not tested.

Note: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

5.5 DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
D032		$\overline{\text{RESET}}$	VSS	—	0.2 VDD	V	4.5V ≤ VDD ≤ 5.5V, otherwise entire range
	VIH	**Input High Voltage**					
D042		$\overline{\text{RESET}}$	0.8 VDD	—	VDD	V	4.5V ≤ VDD ≤ 5.5V, otherwise entire range
	IIL	**Input Leakage Current(2)**					
D060A		Analog inputs	—	±0.1	±1	µA	Vss ≤ VPIN ≤ VDD
D061		$\overline{\text{RESET}}$(1)	—	±1	±5	µA	Vss ≤ VPIN ≤ VDD
		Output Low Voltage					
D080	VOL	Pins LED1, LED2, CTRLOUT, CHGOUT, HVOUT	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	Pins LED1, LED2, CTRLOUT, CHGOUT, HVOUT	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

5.6 DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to +85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D101	CIO	Pins LED1, LED2, CTRLOUT, CHGOUT, HVOUT	—	—	50*	pF	
		Data EEPROM Memory					
D120	ED	Endurance	1M	10M	—	E/W	25°C at 5V
D121	VDRW	VDD for read/write	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

5.7 AC Characteristics: PS200 (Industrial)

FIGURE 5-1: EXTERNAL CLOCK TIMING

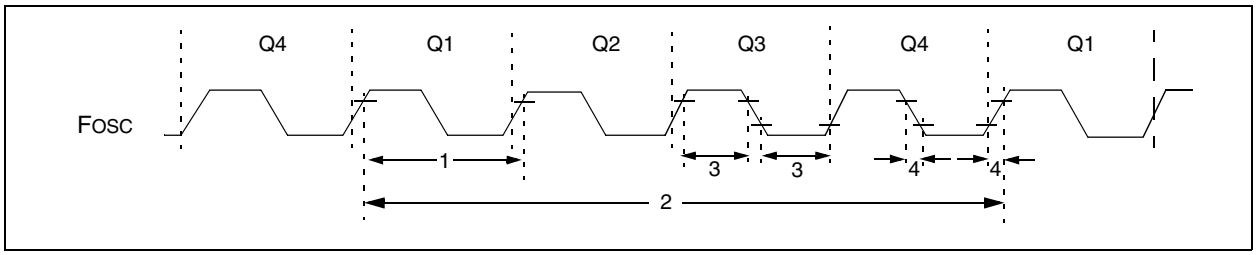


TABLE 5-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	Oscillator Frequency(1)	—	8	—	MHz	Using PS200 internal oscillator
1	TOSC	Oscillator Period(1)	—	125	—	ns	Using PS200 internal oscillator

† Data in “Typ” column is at 5 V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 5-2: CLKO AND I/O TIMING

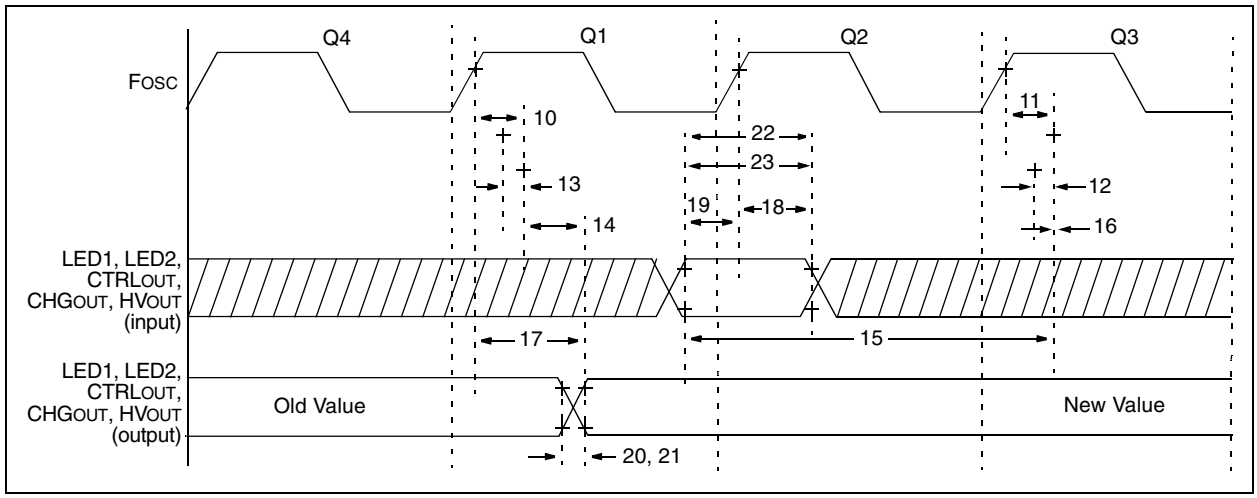


TABLE 5-3: CLKO AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
17	TosH2ioV	FOSC ↑ (Q1 cycle) to Port Out Valid	—	50	150*	ns	
			—	—	300	ns	
18	TosH2ioI	FOSC ↑ (Q2 cycle) to Port Input Invalid (I/O in hold time)	100	—	—	ns	
19	TioV2osH	Port Input Valid to FOSC ↑ (I/O in setup time)	0	—	—	ns	
20	TioR	Port Output Rise Time	—	10	40	ns	
21	TioF	Port Output Fall Time	—	10	40	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0 V, 25°C unless otherwise stated.

FIGURE 5-3: RESET AND POWER-UP TIMER TIMING

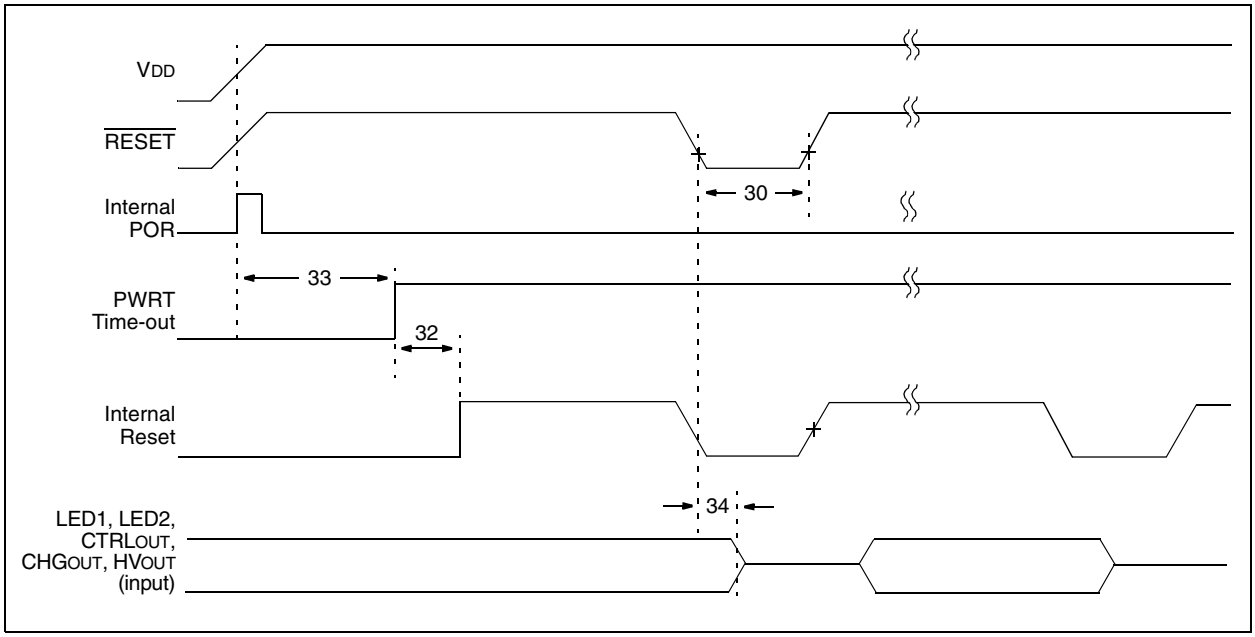


FIGURE 5-4: BROWN-OUT DETECT TIMING AND CHARACTERISTICS

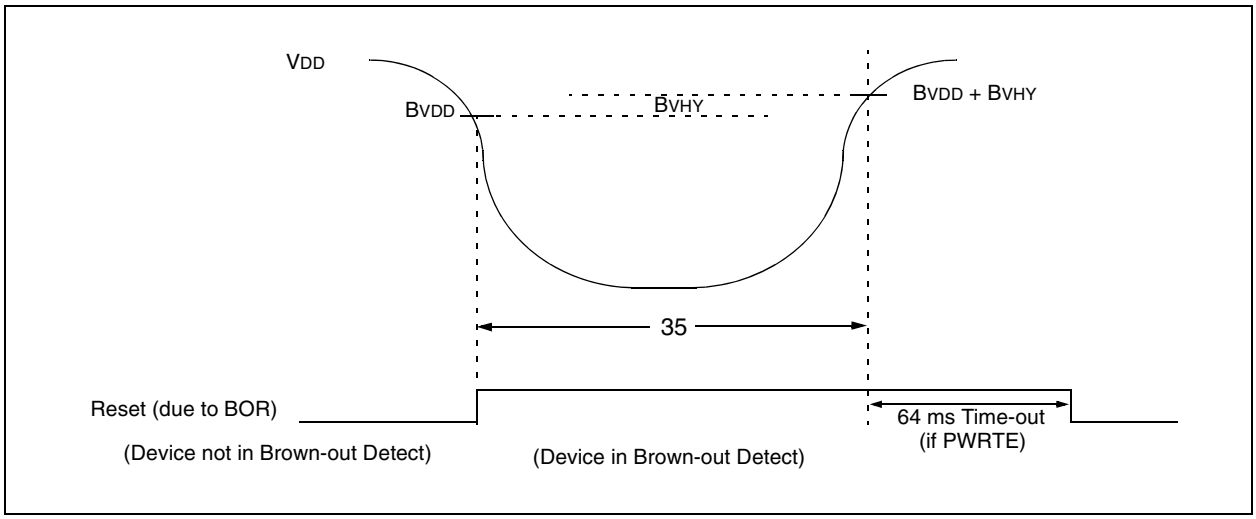


TABLE 5-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT DETECT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCL	$\overline{\text{RESET}}$ Pulse Width (low)	2 11	— 18	— 24	µs ms	VDD = 5V, -40°C to +85°C Extended temperature
32	TOST	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = FOSC period
33*	TPWRT	Power-up Timer Period (4 x TWDT)	28* TBD	64 TBD	132* TBD	ms ms	VDD = 5V, -40°C to +85°C
34	TIOZ	I/O High-Impedance from $\overline{\text{RESET}}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
	BVDD	Brown-out Detect Voltage	2.025		2.175	V	
	BVHY	Brown-out Hysteresis		25		mV	
35	TBOR	Brown-out Detect Pulse Width	100*	—	—	µs	VDD ≤ BVDD (D005)

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 5-5: PRECISION INTERNAL OSCILLATOR PARAMETERS

Param No.	Sym	Characteristic	Freq Tolerance	Min	Typ†	Max	Units	Conditions
F10	FOSC	Internal Calibrated INTOSC Frequency(1)	±1%	—	8.00	TBD	MHz	VDD and Temperature (TBD)
			±2%	—	8.00	TBD	MHz	2.5V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C
			±5%	—	8.00	TBD	MHz	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (Ind.) -40°C ≤ TA ≤ +125°C (Ext.)
F14	TIOSCST	Oscillator Wake-up from Sleep Start-up Time*	—	—	TBD	TBD	µs	VDD = 2.0V, -40°C to +85°C
			—	—	TBD	TBD	µs	VDD = 3.0V, -40°C to +85°C
			—	—	TBD	TBD	µs	VDD = 5.0V, -40°C to +85°C

Legend: TBD = To Be Determined

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and .01 µF values in parallel are recommended.

FIGURE 5-5: CTRLOUT TIMINGS (PIN 5)

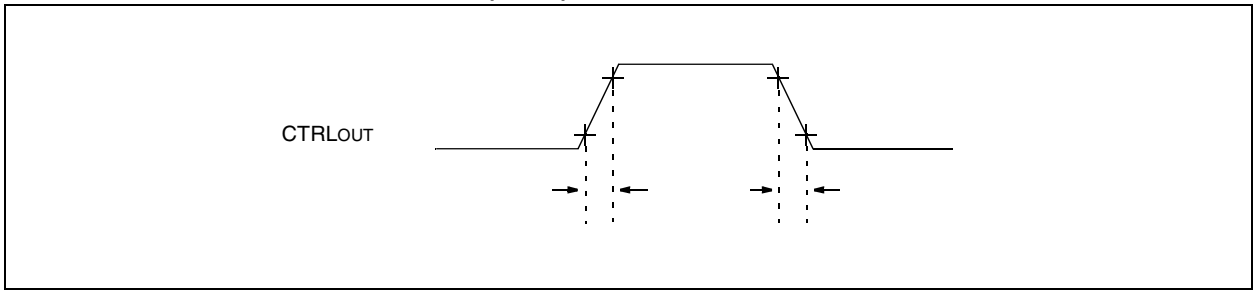


TABLE 5-6: CTRLOUT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
53*	TccR	CTRLOUT Output Rise Time	—	25	50	ns	
54*	TccF	CTRLOUT Output Fall Time	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

5.8 Current Voltage Measurement Block

TABLE 5-7: DC CHARACTERISTICS (PINS LOOPIN, CTRLIN, IFBINB, IFBINA INPUTS; PIN IFBOUT OUTPUT)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) VDD = 2.7V to 5.5V, TA = 25°C, VCM = VDD/2, RL = 100 kΩ to VDD/2 and VOUT ~ VDD/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Sym**	**Parameters**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
001	VOS	**Input Offset Voltage**	—	±5	—	mV	
		Input Current and Impedance					
002	IB	Input Bias Current	—	±2*	—	nA	
003	IOS	Input Offset Bias Current	—	±1*	—	pA	
		Common Mode					
004	VCM	Common Mode Input Range	VSS	—	VDD – 1.4	V	VDD = 5V
005	CMR	Common Mode Rejection	TBD	70	—	dB	VCM = VDD/2, Frequency = DC
		Open-Loop Gain					
006A	AOL	DC Open-Loop Gain	—	90	—	dB	No load
006B	AOL	DC Open-Loop Gain	—	60	—	dB	Standard load
		Output					
007	VOUT	Output Voltage Swing	VSS + 50	—	VDD – 50	mV	TO VDD/2 (20 kΩ connected to VDD,
008	ISC	Output Short Circuit Current	—	25	TBD	mA	20 kΩ + 20 pF to VSS)
		Power Supply					
010	PSR	Power Supply Rejection	80	—	—	dB	

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

TABLE 5-8: AC CHARACTERISTICS (PINS LOOPIN, CTRLIN, IFBINB, IFBINA INPUTS; PIN IFBOUT OUTPUT)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) VDD = 2.7V to 5.5V, VSS = GND, TA = 25°C, VCM = VDD/2, RL = 100 kΩ to VDD/2 and VOUT = VDD/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Sym**	**Parameters**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
011	GBWP	**Gain Bandwidth Product**	—	3	—	MHz	VDD = 5V
012	TON	**Turn-on Time**	—	10	TBD	µs	VDD = 5V
013	ΘM	**Phase Margin**	—	60	—	degrees	VDD = 5V
014	SR	**Slew Rate**	2	TBD	—	V/µs	VDD = 5V

Legend: TBD = To Be Determined

TABLE 5-9: COMPARATOR SPECIFICATIONS (PINS LOOPFBK, CHGFBK, $\overline{SHDN}$, VOVP)

Comparator Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
C01	VOS	Input Offset Voltage	—	± 2	± 5	mV	
C02	VCM	Input Common Mode Voltage	0	—	VDD – 1.5	V	
C03	ILC	Input Leakage Current	—	—	200*	nA	
C04	CMRR	Common Mode Rejection Ratio	+70*	—	—	dB	
C05	TRT	Response Time(1)	— —	— —	20* 40*	ns ns	Internal Output to pin

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD – 1.5V.

TABLE 5-10: COMPARATOR VOLTAGE REFERENCE (VREF) SPECIFICATIONS

Comparator Voltage Reference Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
CV01	CVRES	Resolution	— —	VDD/24* VDD/32	— —	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV02		Absolute Accuracy	— —	— —	±1/4* ±1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03		Unit Resistor Value (R)	—	2K*	—	Ω	
CV04		Settling Time(1)	—	—	10*	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

TABLE 5-11: A/D CONVERTER CHARACTERISTICS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10 bits	bit	
A02	EABS	Total Absolute Error*(1)	—	—	±1	LSb	VREF = 5.0V
A03	EIL	Integral Error	—	—	±1	LSb	VREF = 5.0V
A04	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits, VREF = 5.0V
A05	EFS	Full-Scale Range	2.2*	—	5.5*	V	
A06	EOFF	Offset Error	—	—	±1	LSb	VREF = 5.0V
A07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.0V
A10	—	Monotonicity	—	guaranteed(2)	—	—	VSS ≤ VAIN ≤ VREF
A20 A20A	VREF	Reference Voltage	2.2(4) 2.5	—	— VDD + 0.3	V	 Absolute minimum to ensure 10-bit accuracy
A25	VAIN	Analog Input Voltage	VSS	—	VREF(5)	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
A50	IREF	VREF Input Current*(3)	10 —	— —	1000 10	μA μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes Integral, Differential, Offset and Gain Errors.

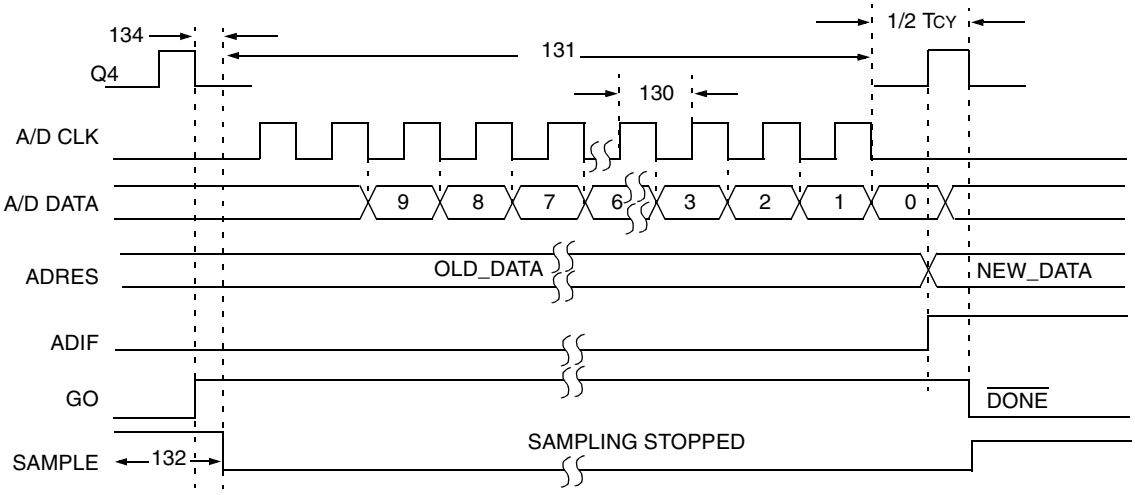
2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: VREF current is from external VREF or VDD pin, whichever is selected as reference input.

4: Only limited when VDD is at or below 2.5V. If VDD is above 2.5V, VREF is allowed to go as low as 1.0V.

5: Analog input voltages are allowed up to VDD, however, the conversion accuracy is limited to VSS to VREF.

FIGURE 5-6: A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 5-12: A/D CONVERSION REQUIREMENTS

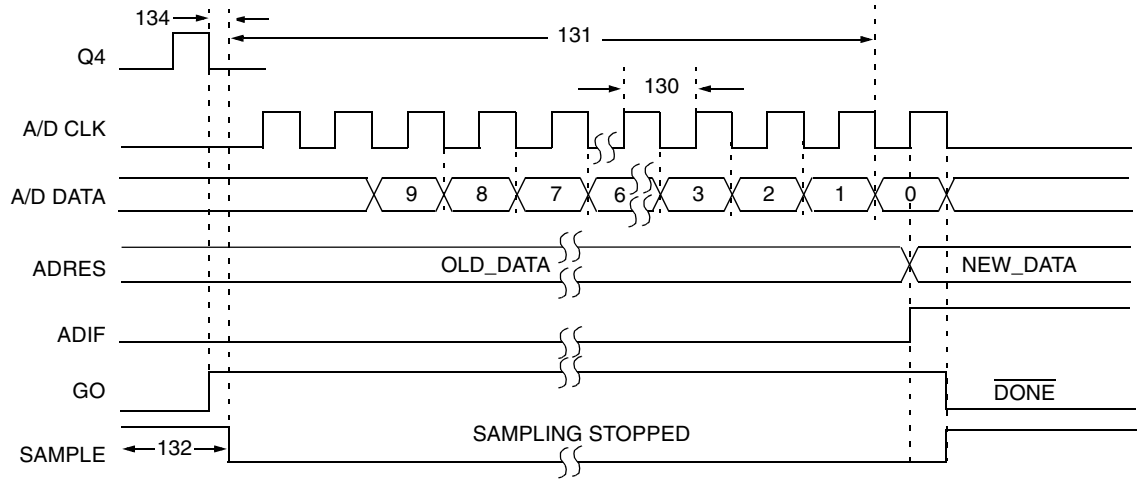
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*	TAD	A/D Clock Period	1.6	—	—	µs	TOSC based, VREF ≥ 2.5V
			3.0*	—	—	µs	TOSC based, VREF full range
130*	TAD	A/D Internal RC Oscillator Period					ADCS<1:0> = 11 (RC mode)
			3.0*	6.0	9.0*	µs	At VDD = 2.5V
			2.0*	4.0	6.0*	µs	At VDD = 5.0V
131*	TCNV	Conversion Time (not including acquisition time)(1)	—	11 TAD	—	TAD	Set GO bit to new data in A/D Result register
132*	TACQ	Acquisition Time	—	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 1 mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D Clock Start	—	TOSC/2	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

FIGURE 5-7: A/D CONVERSION TIMING (SLEEP MODE)



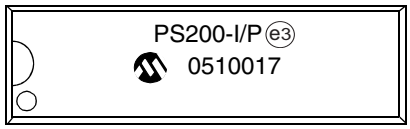
Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

6.0 PACKAGING INFORMATION

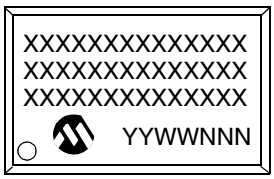
6.1 Package Marking Information

20-Lead PDIP

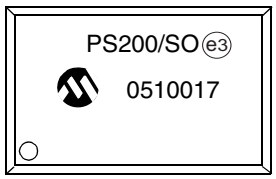
Example



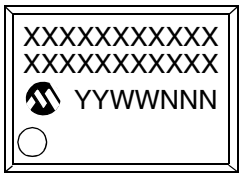
20-Lead SOIC



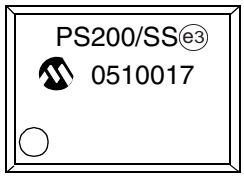
Example



20-Lead SSOP



Example



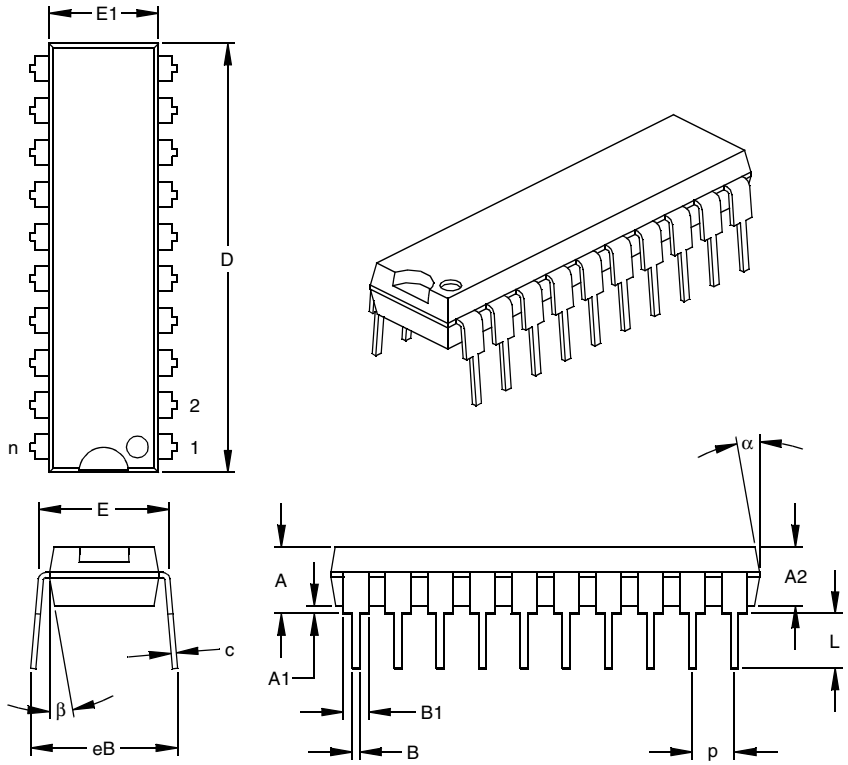
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6.2 Package Details

The following sections give the technical details of the packages.

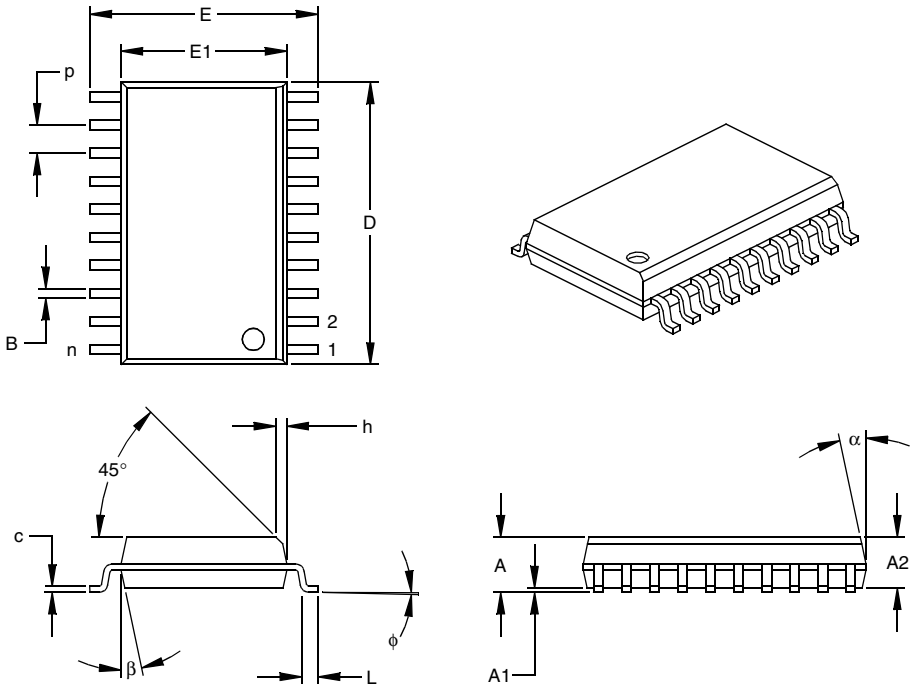
20-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.295	.310	.325	7.49	7.87	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	1.025	1.033	1.040	26.04	26.24	26.42
Tip to Seating Plane	L	.120	.130	.140	3.05	3.30	3.56
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.055	.060	.065	1.40	1.52	1.65
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-019

20-Lead Plastic Small Outline (SO) – Wide, 300 mil Body (SOIC)

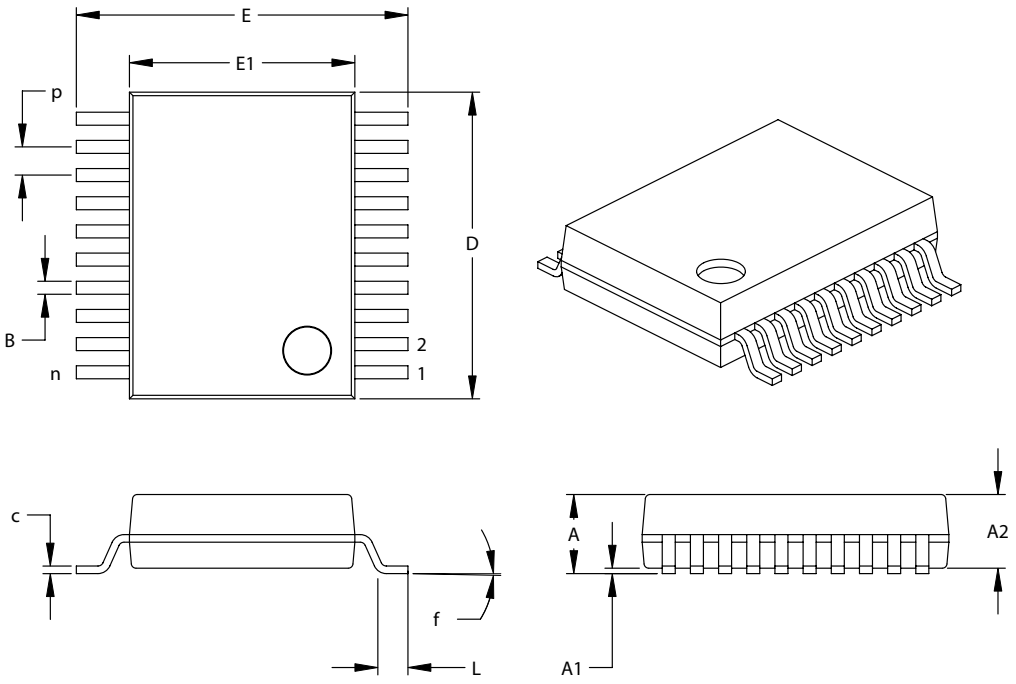


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.496	.504	.512	12.60	12.80	13.00
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-094

20-Lead Plastic Shrink Small Outline (SS) – 209 mil Body, 5.30 mm (SSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	-	-	.079	-	-	2.00
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	-	-	0.05	-	-
Overall Width	E	.291	.307	.323	7.40	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.272	.283	.289	.295	7.20	7.50
Foot Length	L	.022	.030	.037	0.55	0.75	0.95
Lead Thickness	c	.004	-	.010	0.09	-	0.25
Foot Angle	f	0°	4°	8°	0°	4°	8°
Lead Width	B	.009	-	.015	0.22	-	0.38

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-150

Drawing No. C04-072

Revised 11/03/03

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Device	Temperature Range	Package	Pattern

Device	PS200	
Temperature Range	I	= -20°C to +85°C (Industrial)
Package	P	= PDIP
	SO	= SOIC
	SS	= SSOP

Examples:

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